



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,463	11/29/2001	Matthew John Fairhurst	TUC920010104US1	5676

46917 7590 02/09/2005

KONRAD RAYNES & VICTOR, LLP.  
ATTN: IBM37  
315 SOUTH BEVERLY DRIVE, SUITE 210  
BEVERLY HILLS, CA 90212

EXAMINER
----------

BONURA, TIMOTHY M

ART UNIT	PAPER NUMBER
----------	--------------

2114

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/998,463

Applicant(s)

FAIRHURST ET AL.

Examiner

Tim Bonura

Art Unit

2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 05 November 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-64 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4, 9, 13, 16, 18-22, 27, 31, 34, 36-40, 45, 49, 52 and 54 is/are rejected.
- 7) ☒ Claim(s) 5-8, 10-12, 14, 15, 17, 23-26, 28-30, 32, 33, 35, 41-44, 46-48, 50, 51, 53 and 55-63 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

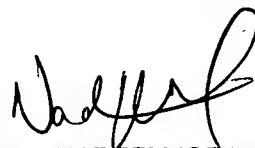
**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 November 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

  
**NADEEM IQBAL**  
**PRIMARY EXAMINER**

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 9, 13, 16, 18-22, 27, 31, 34, 36-40, 45, 49, 52, and 54 are rejected under 35 U.S.C. 102(b) as being anticipated by Powers, et al, U.S. Patent Number 5,212,785.

3. Regarding claim 1:

a. Regarding the limitation of “detecting an error in a system including a first adaptor, wherein the first adaptor is capable of communicating on the storage network after the error is detected,” Powers discloses a system with a plurality of memory devices and components for controlling data flow with failure handling. (Lines 50-55 of Column 1).

b. Regarding the limitation of “determining whether the first adaptor is designated a master of the storage network after the error is,” Powers discloses a system wherein a controller fails and the first control and second controller can handle the fail over and maintain constant configuration of the drives. (Lines 65-68 of Column 3 and Lines 1-5 of Column 4).

c. Regarding the limitation of “starting a master switch timer that is less than a system timeout period if the first adaptor is the master after detecting the error, wherein an error recovery procedure in the system including the first adaptor would be initiated

Art Unit: 2114

after the system timeout period has expired,” Powers discloses a system with a timeout counter for the I/O controller. (Lines 11-14 of Column 7). Once a timeout has occurred, a system failure is indicated and recovery proceeds. (Lines 24-30 of Column 7).

d. Regarding the limitation of “initiating an operation to designate another adaptor in the storage network as the master if the first adaptor is the master in response to detecting an expiration of one started I/O delay timer,” Powers discloses a system with wherein in response to the timeout, a secondary controller takes over as the primary and secondary controller. This is called BOTH STATES by the art. (Lines 65-67 of Column 7 and Line 1 of Column 8).

4. Regarding claim 2, Powers discloses a system wherein a timeout value times out. (Lines 24-27 of Column 7).

5. Regarding claim 3, Powers discloses a system only the controller with the fault shuts down for the fault recovery. (Lines 14-17 of Column 5).

6. Regarding claim 4, Power discloses a system wherein the controller that fails shuts down. It would be inherent that the controller would have to be restarted in order to be brought back online. (Lines 14-17 of Column 5).

7. Regarding claim 9, Powers discloses a system that can start a timeout period after an error detection (Lines 11-14 of Column 7) and releases a controller for the memory device for which it controlled upon the timeout period being reached. (Lines 24-32 of Column 7).

8. Regarding claim 13, Powers discloses a system wherein the secondary controller is a failure for the primary controller. (Lines 30-34 of Column 2).

Art Unit: 2114

9. Regarding claim 16, Power discloses a system wherein the memory devices are shown connected in a loop structure between the two controllers. (See Figure 1, Items 18A, 18B, 18M with 14A and 14B).

10. Regarding claim 18, Powers discloses system wherein the controller can suffer a complete failure, which results in total lack of communication with the memory devices. (Lines 23-27 of Column 2).

11. Regarding claim 19:

e. Regarding the limitation of “a second adaptor capable of communicating on the storage network,” Powers discloses a system with a second controller. (Lines 66-67 of Column 1 and Lines 1-5 of Column 2).

f. Regarding the limitation of “detecting an error in a system including a first adaptor, wherein the first adaptor is capable of communicating on the storage network after the error is detected,” Powers discloses a system with a plurality of memory devices and components for controlling data flow with failure handling. (Lines 50-55 of Column 1).

g. Regarding the limitation of “determining whether the first adaptor is designated a master of the storage network after the error is,” Powers discloses a system wherein a controller fails and the first control and second controller can handle the fail over and maintain constant configuration of the drives. (Lines 65-68 of Column 3 and Lines 1-5 of Column 4).

h. Regarding the limitation of “starting a master switch timer that is less than a system timeout period if the first adaptor is the master after detecting the error, wherein

an error recovery procedure in the system including the first adaptor would be initiated after the system timeout period has expired,” Powers discloses a system with a timeout counter for the I/O controller. (Lines 11-14 of Column 7). Once a timeout has occurred, a system failure is indicated and recovery proceeds. (Lines 24-30 of Column 7).

- i. Regarding the limitation of “initiating an operation to designate another adaptor in the storage network as the master if the first adaptor is the master in response to detecting an expiration of one started I/O delay timer,” Powers discloses a system with wherein in response to the timeout, a secondary controller takes over as the primary and secondary controller. This is called BOTH STATES by the art. (Lines 65-67 of Column 7 and Line 1 of Column 8).
12. Regarding claim 20, Powers discloses a system wherein a timeout value times out. (Lines 24-27 of Column 7).
13. Regarding claim 21, Powers discloses a system only the controller with the fault shuts down for the fault recovery. (Lines 14-17 of Column 5).
14. Regarding claim 22, Power discloses a system wherein the controller that fails shuts down. It would be inherent that the controller would have to be restarted in order to be brought back online. (Lines 14-17 of Column 5).
15. Regarding claim 27, Powers discloses a system that can start a timeout period after an error detection (Lines 11-14 of Column 7) and releases a controller for the memory device for which it controlled upon the timeout period being reached. (Lines 24-32 of Column 7).
16. Regarding claim 31, Powers discloses a system wherein the secondary controller is a failure for the primary controller. (Lines 30-34 of Column 2).

Art Unit: 2114

17. Regarding claim 34, Power discloses a system wherein the memory devices are shown connected in a loop structure between the two controllers. (See Figure 1, Items 18A, 18B, 18M with 14A and 14B).

18. Regarding claim 36, Powers discloses system wherein the controller can suffer a complete failure, which results in total lack of communication with the memory devices. (Lines 23-27 of Column 2).

19. Regarding claim 37:

j. Regarding the limitation of “detecting an error in a system including a first adaptor, wherein the first adaptor is capable of communicating on the storage network after the error is detected,” Powers discloses a system with a plurality of memory devices and components for controlling data flow with failure handling. (Lines 50-55 of Column 1).

k. Regarding the limitation of “determining whether the first adaptor is designated a master of the storage network after the error is,” Powers discloses a system wherein a controller fails and the first control and second controller can handle the fail over and maintain constant configuration of the drives. (Lines 65-68 of Column 3 and Lines 1-5 of Column 4).

l. Regarding the limitation of “starting a master switch timer that is less than a system timeout period if the first adaptor is the master after detecting the error, wherein an error recovery procedure in the system including the first adaptor would be initiated after the system timeout period has expired,” Powers discloses a system with a timeout

Art Unit: 2114

counter for the I/O controller. (Lines 11-14 of Column 7). Once a timeout has occurred, a system failure is indicated and recovery proceeds. (Lines 24-30 of Column 7).

m. Regarding the limitation of “initiating an operation to designate another adaptor in the storage network as the master if the first adaptor is the master in response to detecting an expiration of one started I/O delay timer,” Powers discloses a system with wherein in response to the timeout, a secondary controller takes over as the primary and secondary controller. This is called BOTH STATES by the art. (Lines 65-67 of Column 7 and Line 1 of Column 8).

20. Regarding claim 38, Powers discloses a system wherein a timeout value times out. (Lines 24-27 of Column 7).

21. Regarding claim 39, Powers discloses a system only the controller with the fault shuts down for the fault recovery. (Lines 14-17 of Column 5).

22. Regarding claim 40, Power discloses a system wherein the controller that fails shuts down. It would be inherent that the controller would have to be restarted in order to be brought back online. (Lines 14-17 of Column 5).

23. Regarding claim 45, Powers discloses a system that can start a timeout period after an error detection (Lines 11-14 of Column 7) and releases a controller for the memory device for which it controlled upon the timeout period being reached. (Lines 24-32 of Column 7).

24. Regarding claim 49, Powers discloses a system wherein the secondary controller is a failure for the primary controller. (Lines 30-34 of Column 2).

Art Unit: 2114

25. Regarding claim 52, Power discloses a system wherein the memory devices are shown connected in a loop structure between the two controllers. (See Figure 1, Items 18A, 18B, 18M with 14A and 14B).

26. Regarding claim 54, Powers discloses system wherein the controller can suffer a complete failure, which results in total lack of communication with the memory devices. (Lines 23-27 of Column 2).

***Allowable Subject Matter***

27. Claims 5-8, 10-12, 14-15, 17, 23-26, 28-30, 32-33, 35, 41-44, 46-48, 50-51, 53 and 55-63 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Response to Arguments***

28. Applicant's arguments see response to non-final rejection, filed 11/05/2004, with respect to claims 24 and 37 have been fully considered and are persuasive. The rejections/objects of claims 24 and 37 have been withdrawn.

29. Applicant's arguments filed 11/05/2004 have been fully considered but they are not persuasive.

30. Regarding the arguments for claim 1:

n. The applicant argues that the prior art of record does not teach "designating another adaptor as the master if the first adaptor is the master, in response to detecting an

Art Unit: 2114

expiration of the master switch timer that is less than a system timeout period.” The examiner contends that the prior art of record does teach a timeout period and designating a second controller as the “master” controller. The prior art of record being Powers, et al, U.S. Patent Number 5,212,785.

o. Concerning the arguments of the master controller, the examiner contends (see Lines 12-39 of Column 2), that Powers describes what one skilled in the art would consider a the designation of a master controller. One controller of a set of controllers, which is communicating with a set of memory devices, fails. A redundant controller then receives a message indicating the failure, notifies the first level controllers of the error, and the data paths are switched to the properly work controller. The examiner contends that this covers the claimed limitation.

p. Concerning the argument of the system timeout period. The examiner contends that the prior art of record does teach a timeout period less than the system timeout period. The prior art of record states that on possible failover situations, as described further (Lines 17-33 of Column 8), results in a failover after a timer was set, and for the complete failover to occur without interruption to the operations of the computer system. (Lines 27-36 of Column 5). The examiner contends that this signifies that the failover occurs in less time than the system would typically process I/O or messages to the memory devices. Therefore the prior art of record does teach a system with a timeout period less than the system timeout period.

31. Regarding the arguments for claims 19 and 37 please refer to the response to the arguments for claim 1. (paragraph 36, above).

Art Unit: 2114

32. Regarding the arguments for claims 2-18, 20-36, and 38-54, since no further arguments are made over the prior art and the claims all depend from 1, 19, or 37, the rejections stand.

### ***Conclusion***

33. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tim Bonura**.

- The examiner can normally be reached on **Mon-Fri: 8:30-5:00**.
- The examiner can be reached at: **571-272-3654**.

35. If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, **Rob Beausoliel**.

- The supervisor can be reached on **571-272-3645**.

Art Unit: 2114

36. The fax phone numbers for the organization where this application or proceeding is assigned are:

- **703-872-9306 for all patent related correspondence by FAX.**

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov/>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

38. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **receptionist** whose telephone number is: **571-272-2100**.

39. Responses should be mailed to:

- **Commissioner of Patents and Trademarks**

**P.O. Box 1450**

**Alexandria, VA 22313-1450**



NADEEM IQBAL  
PRIMARY EXAMINER  
tmb  
February 1, 2005

Tim Bonura  
Examiner  
Art Unit 2114